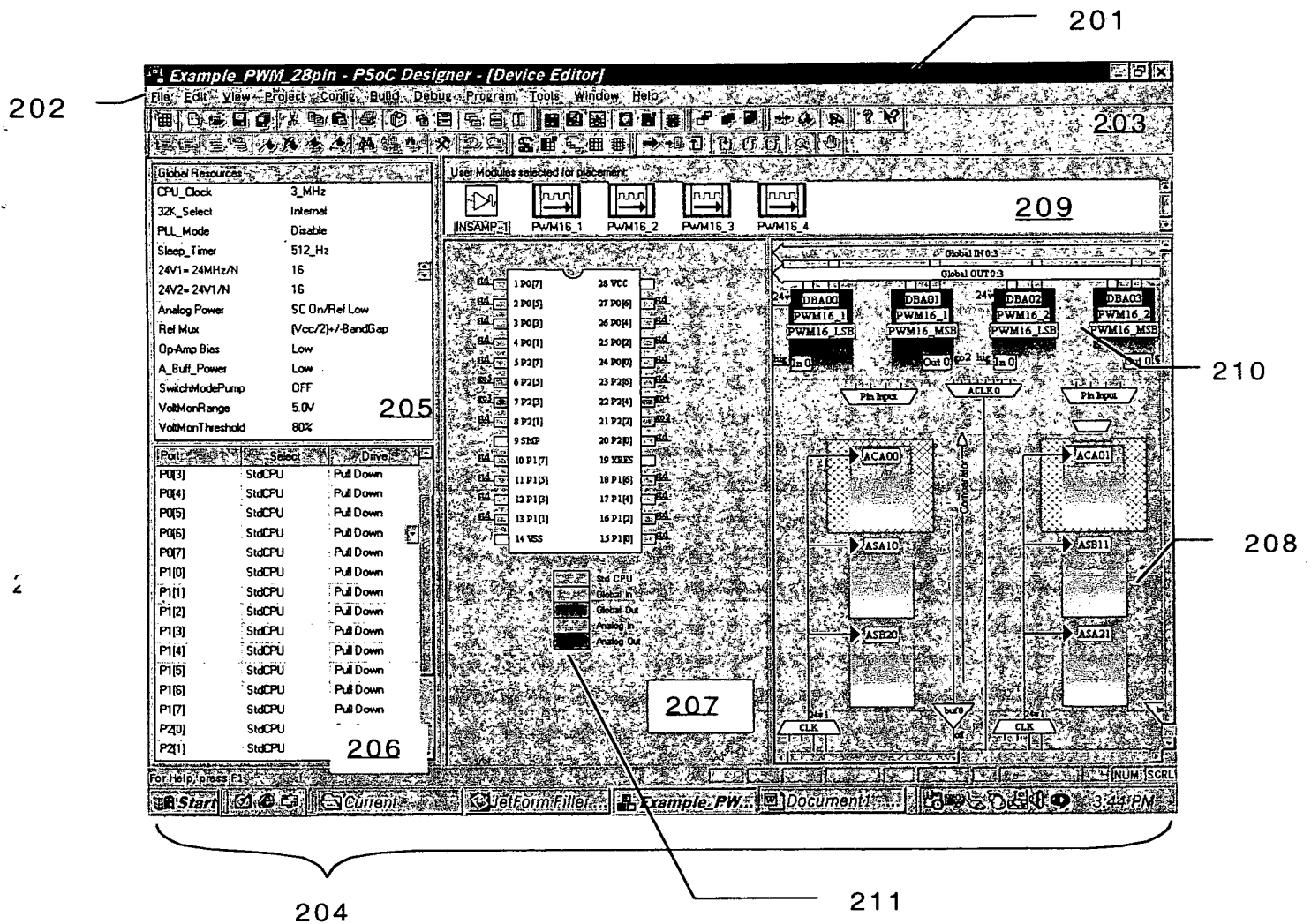


**FIGURE 1** BEST AVAILABLE COPY

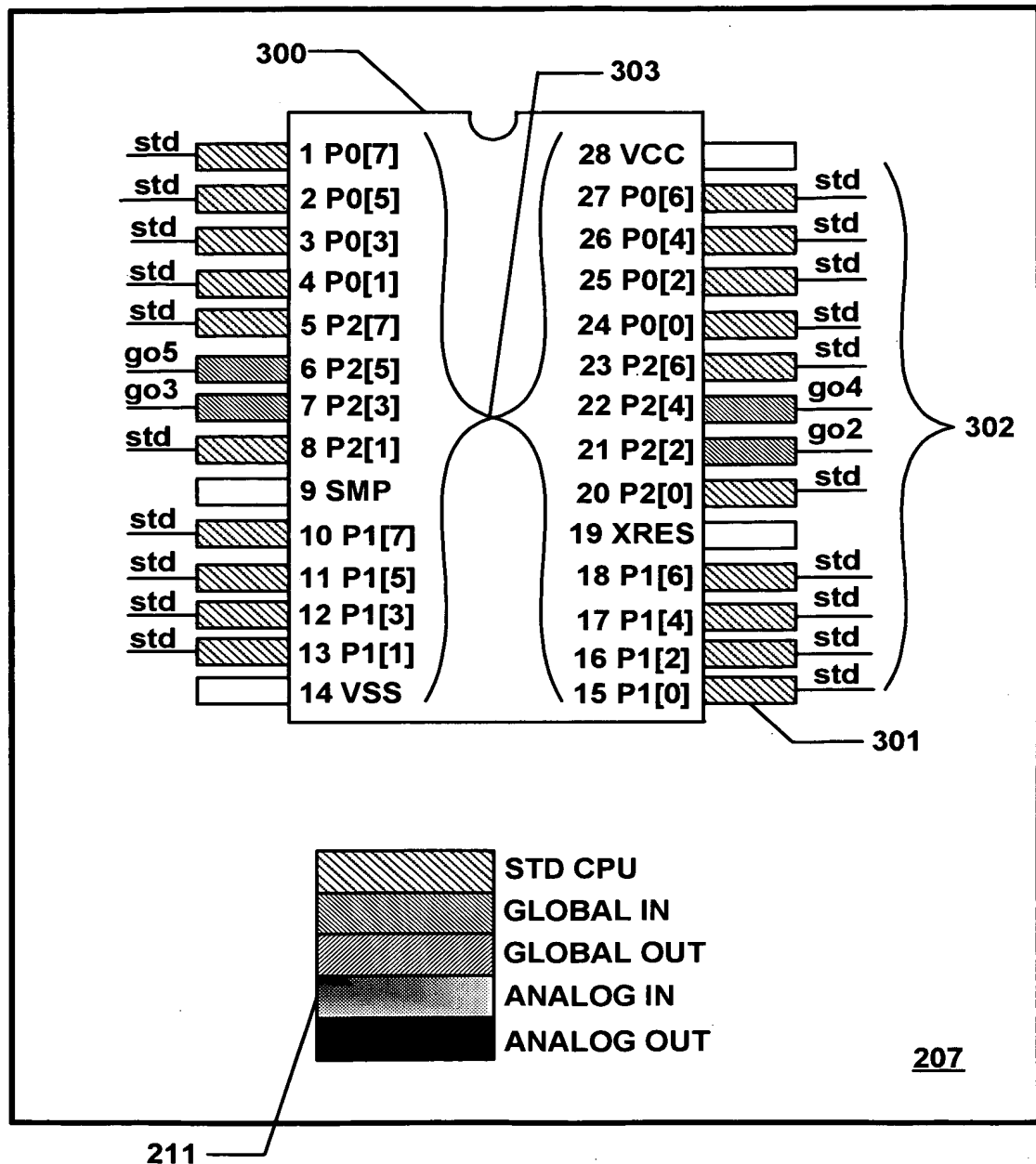
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FIGURE 2

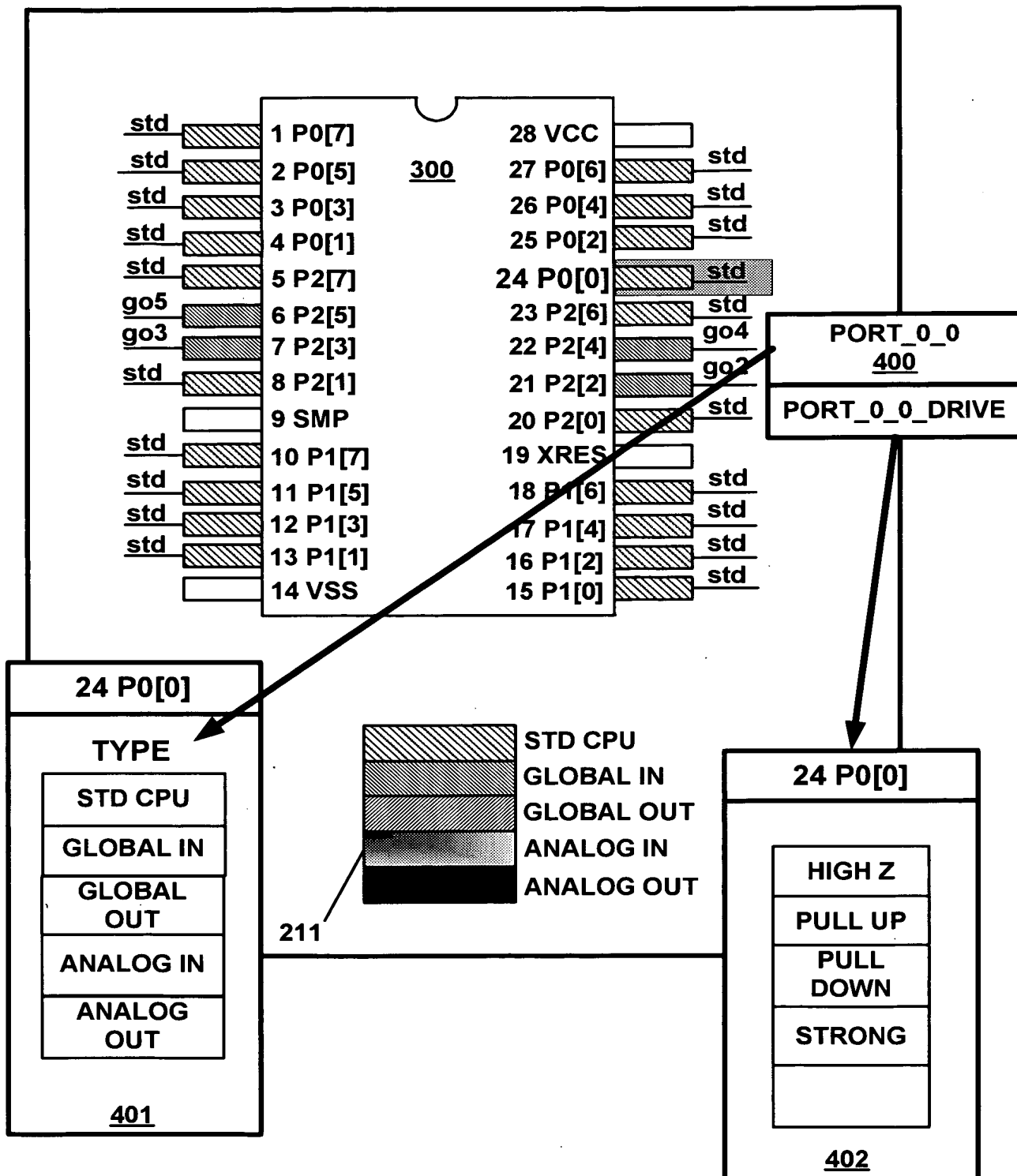
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FIGURE 3

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FIGURE 4

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PORT	SELECT	DRIVE
P0 [0]	StdCPU	HIGH Z
P0 [1]	StdCPU	PULL DOWN
P0 [2]	StdCPU	PULL DOWN
P0 [3]	StdCPU	PULL DOWN
P0 [4]	StdCPU	PULL DOWN
P0 [5]	StdCPU	PULL DOWN
P0 [6]	StdCPU	PULL DOWN
P0 [7]	StdCPU	PULL DOWN
P1 [0]	StdCPU	PULL DOWN
P1 [1]	StdCPU	PULL DOWN
P1 [2]	StdCPU	PULL DOWN
P1 [3]	StdCPU	PULL DOWN
P1 [4]	StdCPU	PULL DOWN
P1 [5]	StdCPU	PULL DOWN
P1 [6]	StdCPU	PULL DOWN
P1 [7]	StdCPU	PULL DOWN
P2 [0]	StdCPU	PULL DOWN
P2 [1]	GLOBAL OUT	PULL DOWN
P2 [2]	GLOBAL OUT	PULL DOWN
P2 [3]	GLOBAL OUT	PULL DOWN

502

506

505

504

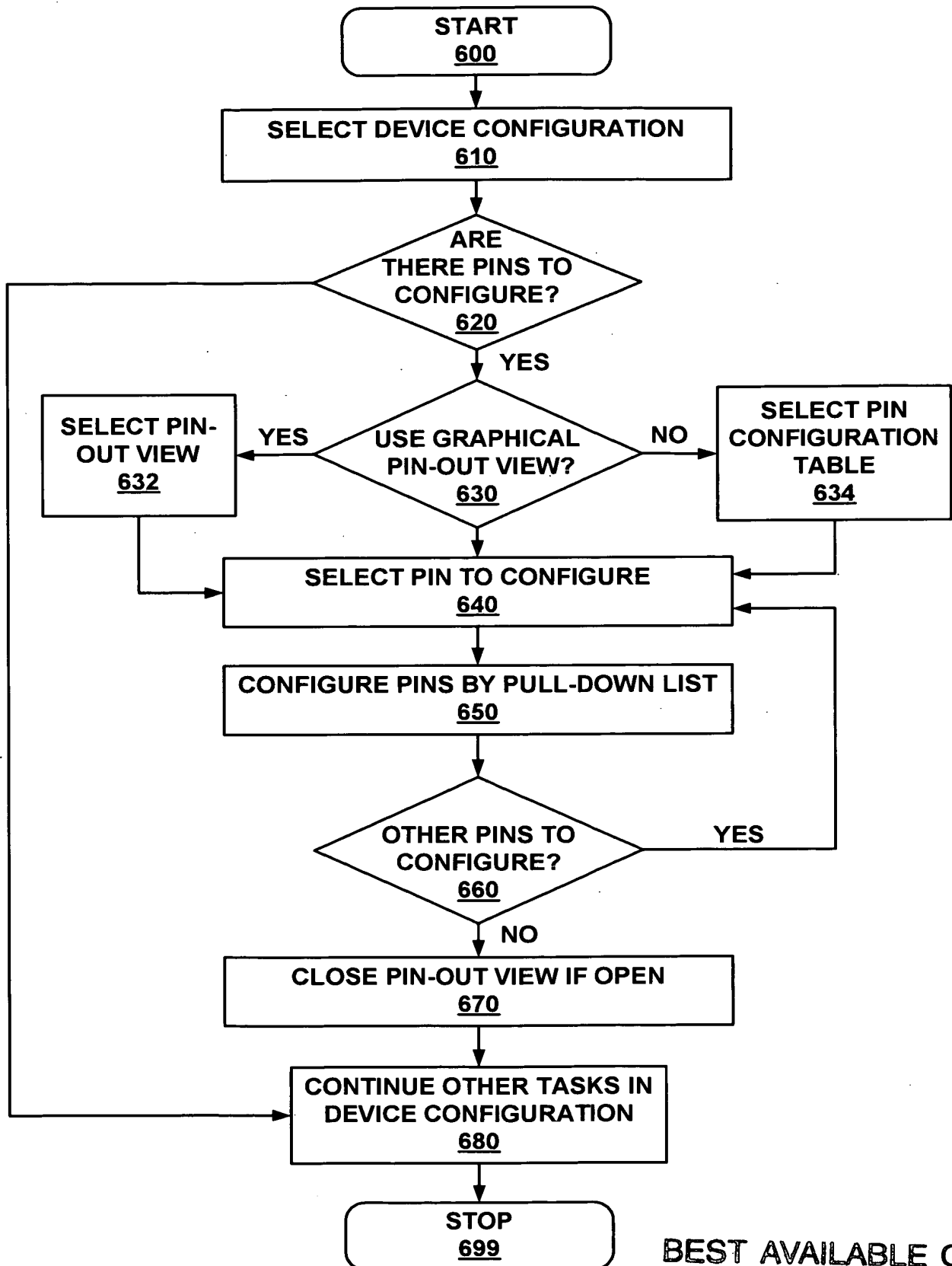
503

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**FIGURE 5**

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**FIGURE 6**